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A Novel Modular Multilevel Inverter Circuit for High Voltage Power Transmission Application

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Abstract—*This paper proposed an improved phase disposition pulse width modulation (PDPWM) for a modular multilevel inverter which is used for Photovoltaic grid connection. This new modulation method is based on selective virtual loop mapping, to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. The concept of virtual sub module (VSM) is first established, and by changing the loop mapping relationships between the VSMs and the real submodules, the voltages of the upper/lower arm's capacitors can be well balanced. This method does not requiring sorting voltages from highest to lowest, and just identifies the MIN and MAX capacitor voltage's index which makes it suitable for a modular multilevel converter with a large number of submodules in one arm. Compared to carrier phase-shifted PWM (CPSPWM), this method is more easily to be realized field - programmable gate array and has much stronger dynamic regulation ability, and is conducive to the control of circulating current. Its feasibility and validity have been verified by simulations and experiments.*

1. INTRODUCTION

In recent years, with the development of a large-scale photovoltaic (PV) power plant system, as well as smart grid and multilevel technologies, higher requirements in volt- age level, modular structure, and flexibility and reliability of the next-generation large-scale PV grid-connected inverter have been put forward. The features include the following:

1) Power peaking capacity: PV systems should be able to store the electrical energy which is issued by itself as needed during light load conditions; meanwhile, this part of electrical energy would be released again for the load when the load is at the peak. As a result, the peak power of the grid and the reliability of power supply can be improved.

2) Fault ride-through capacity: A large-scale PV system has been required to have the ability to withstand short periods of voltage abnormality, such as the voltage short-term drop caused by short-circuit fault. The PV system

Should maintain the connection of the inverter and the grid in addition to providing support to the grid.

3) Power quality control: More stable power supply performance could be achieved by introducing suitable inverter control strategy including voltage stability, phase regulation, active filter etc.

4) Higher redundancy and error correction capacity: The PV system should have the capacity to work efficiently when the failure occurs in some of the modules of the inverter system and should be "smart" enough to correct the situation.

The MMC used in the PV grid-connected system is just mentioned in the literature survey.

The reasons of this situation are as follows:

1) MMC related research is mostly in theoretical research stage in the literature survey.

2) The characteristic of the photovoltaic power generation is that PV panels are intermittent sources, and their output voltages continuously vary the dc link's voltage has to be regulated to keep them working in maximum power point tracking (MPPT) status.

3) The dynamic voltage balance has to be considered in multilevel PWM, while the system stability would be damaged by adding improper signals to the reference voltage in the literature survey.

4) The unique circulating current of the MMC will increase the system losses and is not conducive for improving the efficiency of the inverter output in the literature survey and the most important point is that the uncontrolled circulating current threatens the stability of the MMC.

A new selective virtual loop mapping (SVLM) method based on phase disposition PWM (PDPWM) which has voltage balance capability is proposed here. The concept of virtual submodules (VSM) is established, and by changing the mapping routines between the VSM and the real submodules (RSM) with SVLM, the capacitor voltages of the upper and

lower arms can be balanced even if the inverter loses its symmetry.

The method has been designed to consider the following situations:

1) No extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current.

2) The possibility of a large number of submodules in one arm.

3) Retain equivalent switching frequency of the PDPWM.

4) It could be easily realized infield programmable gate array (FPGA) for a large-scale converter which has a large number of sub modules.

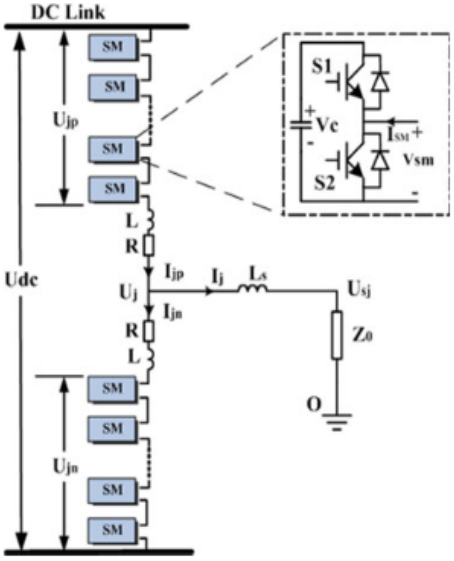


Fig. 1.1: Single-phase equivalent circuit of a multilevel converter.

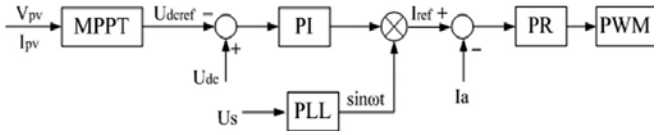


Fig. 1.2: Control scheme of the single-phase PV grid-connected inverter.

2. MODULAR MULTILEVEL PV INVERTER

2.1 MODULATION PRINCIPLES

Fig.1.1 shows the single-phase equivalent circuit of the MMC, which has two arms including the upper arm and the lower arm, with each arm having *N* submodules (SM), one buffer inductor *L*, and equivalent resistor *R*. The dc link of the MMC is floated or connected to high-voltage sources depending on the working purpose of the converter.

The output of the converter is the connection point of the upper and lower arms. *L* is the ac-link inductor, and Z_0 is the equivalent impedance of the ac side. The working states of SM are shown in Table I. Each SM has two states ("ON" and "OFF"), and the corresponding output voltage (U_{sm}) of the SM is V_c or 0. The capacitor will charge or discharge during the period of the "ON" state of the SM depending on the direction of Ism. For example if $I > 0$ the capacitor would be charged, and if $I < 0$, the capacitor would be discharged. The capacitor voltage will be kept while the SM is "OFF."

Table I: Half-Bridge Submodule Working States

mode	S1	S2	Usm	Ism	state	capacitor
1	1	0	Vc	>0	on	Charging
2	1	0	Vc	<0	on	discharging
3	0	1	0	>0	off	Unchanged
4	0	1	0	<0	off	Unchanged

2.2 Basic Structure and Control

There are two structures which can be used in medium- and high-voltage PV grid-connected inverters with MMC: single-stage and two-stage structures. The series-connected PV modules of a single-stage structure access the dc link directly, while in a two-stage structure the procedure is different: PV panels could be connected to the dc link by cascaded dc/dc circuits. The differences are that voltage ripples of the single-stage structure are bigger than those of the two-stage structure, and the two-stage structure has more complex control.

Fig. 2.1 shows the control block diagram of a modular multilevel PV inverter where U_{dcref} the reference of the dc-link voltage is and U_{dc} is the real dc-link voltage they are compared with each other to produce the active reference current i_{dref} after the PI controller. $i_{q\,ref}$ is the reactive reference current. U_s (a, b, c) is the ac-side grid voltage and $I\ (a, b, c)$ is the output current of the MMC. $S\,j\ (1, \ldots, 2N, j = a, b, c)$ are the PWM signals of the MMC.

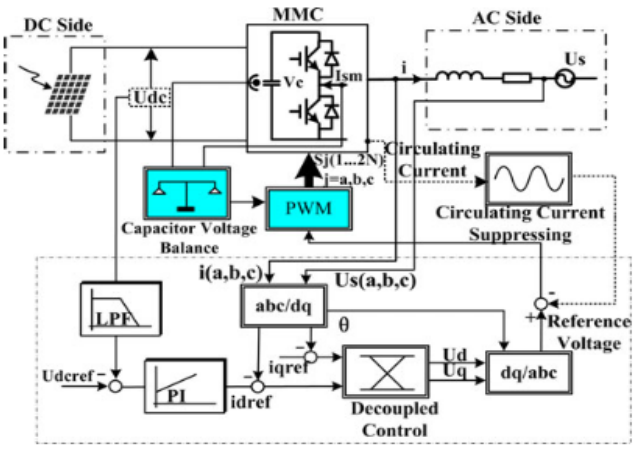


Fig. 2.1: Modular multilevel PV inverter overall control block diagram.

It can be seen that the reference voltage can be acquired by decoupled control and the circulating current suppression compensation signal should be added to it. Meanwhile it is no longer possible to balance the system capacitor voltage dynamically by generating the appropriate balance compensation signal but solely by the adjustment of the PWM method. This approach has the advantage of not only avoiding excessive compensation signal mutual interference (which increases system stability), but also provides a good basis for circulating current suppression and promotes high dc voltage utilization ratio.

3. PHASE DISPOSITION PWM METHOD

As an important modulation method, carrier disposition (CD) PWM has been widely used in multilevel modulation, and it can be divided into three types: phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). For simplicity, this paper will focus on the PDPWM to discuss MMC modulation. PDPWM has been studied for MMC modulation in order to balance capacitor voltages, rotating carrier waves were used, but it seems that they can only work under symmetric condition.

For convenience, it is assumed that the number of RSMs of the upper and lower arms is 4

(N = 4). And the RSMs are numbered from 1 to 8 (from top to bottom).To improve the PDPWM, the concept of VSM can be first established, which means that the VSMs are not the RSMs, and the PWM output gained by the comparison of the modulation signals and the carriers will be transferred to the VSM atfirst, and VSMs are numbered by $1'$ to $2N'$. The transfer relationships are illustrated as Figs. 3.1 and 3.2.

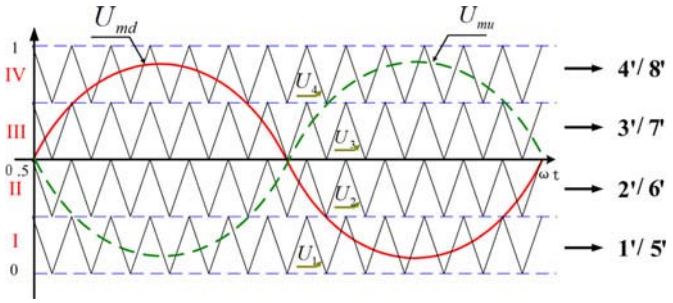


Fig. 3.1: Transfer relationships of VSM.

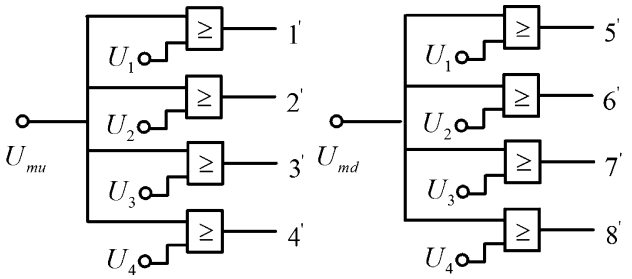


Fig. 3.2: VSM's input.

According to Figs. 3 and 4, 2N + 1 level modulation truth table can be shown as in Table I. $1'$ to $4'$ are for the upper arm's VSMs, while $5'$ to $8'$ represent the lower arm's VSMs. Here, "1" means that the corresponding VSM is ON while "0" means that it is OFF.

Table I: Switch combinations of vsm (2n + 1level)

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	0	0	0	0 ~ 0.25
II	1	P2	0	0	1	P6	0	0	0.25 ~ 0.5
III	1	1	P3	0	1	1	P7	0	0.5~ 0.75
IV	1	1	1	P4	1	1	1	P8	0.75 ~ 1

P1–P8 is the corresponding PWM signal of each VSM's input.

P1–P4 are the comparison results of the carriers and the modulation signals. The range of normalized voltage corresponds to Regions I–IV. In each region, each VSM has its own PWM signal. Compared with Table I; the driving signals of the lower arm's VSMs are complementary to the upper arm.

Table II: Shows the N + 1 level modulation

Region	1'	2'	3'	4'	5'	6'	7'	8'	Range of Normalized Voltage
I	P1	0	0	0	P5	1	1	1	0 ~ 0.25
II	1	P2	0	0	0	P6	1	1	0.25 ~ 0.5
III	1	1	P3	0	0	0	P7	1	0.5~ 0.75
IV	1	1	1	P4	0	0	0	P8	0.75 ~ 1

P5– P8 is the corresponding negated PWM signal of P1~P4 respectively.

Because the 2N + 1 level modulation has higher dc-link voltage ripple, here we choose the N + 1 level modulation as the PV grid-connected inverter's modulation method. The driving signals of VSMs would be transferred to the RSM by certain mapping rules.

4. CAPACITOR VOLTAGE VIRTUAL LOOP MAPPING BALANCE CONTROL

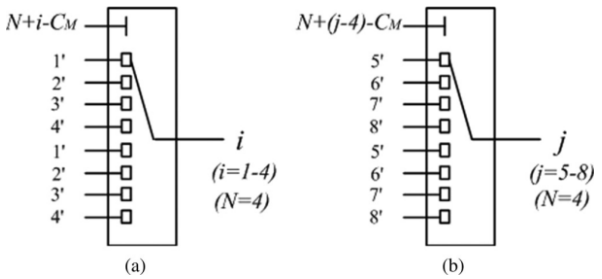
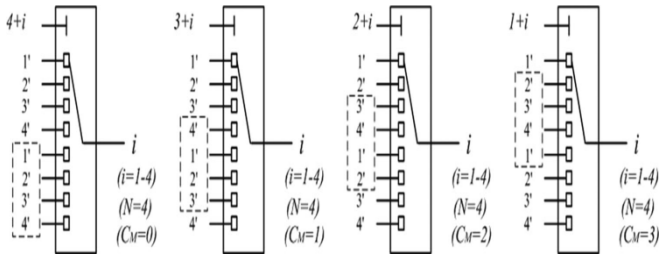


Fig. 4.1: VLM's mapping relationship. (a) Upper arm's mapping. (b) Lower arm's mapping.

To solve the sub-module capacitor voltage balance control problems, there are two mechanisms: the virtual loop mapping (VLM) method and the enhanced SVLM based on the comparison of capacitor voltage MIN and MAX values.



4.2 Upper arm's VLM procedures.

The VLM's principle is using a count-up counter C_M to control the mapping relationships between the VSMs and the RSMs. The C_M working frequency can be set equal to the carrier frequency or less, and its counting range is $0-(N-1)$. Different counter number means different mappings. The VLM can be realized easily by using multiplexer with single-pass transistor in FPGA like Fig. 4.2 (N = 4); the double input buffer (DIB) structure is also used here.

i And j in Fig.4.1 are the index numbers of the RSM, respectively, which work with the counter to realize the mapping between the VSMs and the RSMs. For example, if $C_M = 0$, $N+i-C_M = 4+i-0 = 4+i$ VSMs $1'-2'-3'-4'$ would be mapped to RSMs 1-2-3-4 as shown in Fig. 3.5(a); likewise if $C_M = 1$ $N+i-C_M = 4+i-1 = 3+i$ VSMs $4'-3'-2'-1'$ would be mapped to RSMs 1-2-3-4 [see Fig. 4.3(b)], and so on.

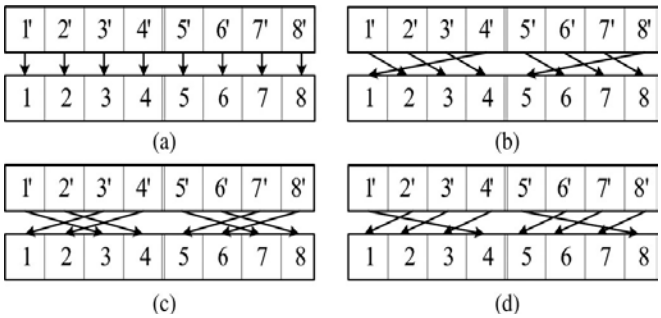


Fig. 4.3: VLM final results: (a) $C_M = 0$ (b) C_M =1(c) $C_M = 2$(d) $C_M = 3$

The VLM's final results of both arms are illustrated in Fig. 4.3. This method can achieve capacitor voltage balance in the case of system symmetry.

5. CAPACITOR VOLTAGE SVLM BALANCE CONTROL

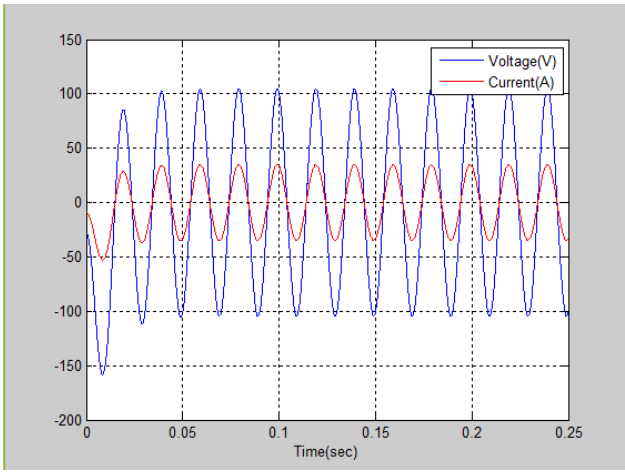
A practical modulation method should not only be effective in a symmetrical system, but also have the ability to regulate dynamically and provide some error correction capabilities to ensure that the system works well under conditions such as error accumulation and device parameter deviation. For example, commonly used phase-shift PWM, by changing the modulation signals of the upper and lower arms to get the dynamic balance adjustment capacity of the capacitor voltage, will bring more harmonics to the arm current, change the circulating current characteristics, and may cause instability. Therefore, changing the modulation signals to achieve the dynamic adjustment capability would be valid only to a certain extent.

The new method is mainly through the SVLM to achieve the effect of dynamic regulation ability; here, "selective" means just taking out the capacitor voltage of MIN and MAX values and their corresponding index selectively. Before introducing the SVLM rules, note that there are four interesting SMs in Table II which are 1', 4', 5' and 8'. VSMs 1' and 8' output PWM in regions I and IV respectively, and output "1" in other regions. Likewise, VSMs 4' and 5' output PWM in regions IV and I, and output "0" in other regions. Table III shows that if some capacitor voltage of the leg is less than the others (i.e. needs more charging and less discharging), it would be right to map the SMs 1' and 8' to this sub-module when the corresponding current *Ism* is positive and mapping the SMs 4' and 5' to it when *Ism* is negative.

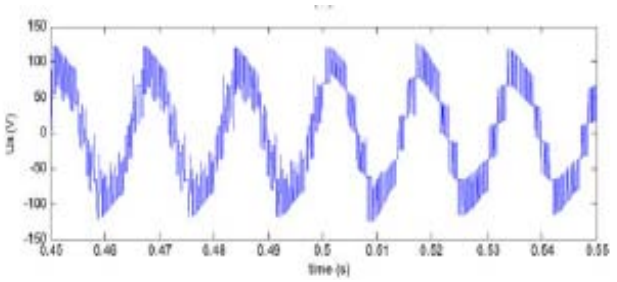
To achieve the SVLM, it needs to sort the capacitor voltage, but frequent sorting is very time consuming, and requires more hardware resources, which would be a large burden especially for high-voltage applications needing more submodules. Other disadvantages of sorting are a reduction in system equivalent frequency and an increase in switching losses. Therefore, the actual method of selective mapping in this paper is just picking the MIN and MAX capacitor voltages and their corresponding index directly and make sure that it can be easily implemented in FPGA.

6. SIMULATION RESULTS

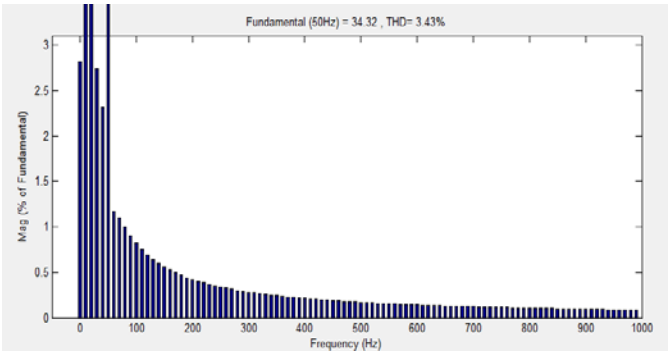
Modular multilevel inverter output waveforms.



(a) System voltage and output current



(b) Inverter output voltage



(c) Harmonics of Output Current

7. CONCLUSION

This paper first discussed the possibilities of the MMC being used as an interface between the grid and PV panels, and proposed an improved SVLM method based on the PD PWM. This method can produce $2N + 1$ and $N + 1$ level outputs in the MMC, and achieve sub module capacitor voltage dynamic balance compensation control while not changing the reference signal. The whole mapping rules are presented and it is easy to be implemented in FPGA.

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